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Technical Performance Report

**SUPERCONDUCTING/SEMICONDUCTING HYBRIDS AND
ADVANCE MEMORY CONCEPTS FOR SUPERCONDUCTING
ELECTRONICS**

ONR Grant N00014-92-J-1886

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Stanford University
29 March 1994

The goal of this program is to explore advance alternatives to the standard approaches to memory in Josephson junction digital electronics. The work includes the systems, circuits and materials aspects of the problem.

INTRODUCTION

It is widely recognized that memory is the weak suit of digital superconductive electronics. Present concepts based on storage of magnetic flux quanta have large cells, are hard to build, and put very severe constraints on the tolerances for the critical currents of the junctions. Previously we have investigated two approaches to reducing the size of the cells: kinetic inductance memory cells and ferromagnetic cores in the conventional cells. While both lead to reduced size and potentially greater speed, they do not alleviate the fabrication tolerance problems. Hence, they do not provide a good solution that can be built with present fabrication capabilities. Given the difficulties with all superconducting approaches we have begun to look at hybrid approaches. Primarily this has involved examination of the issues associated with using cold CMOS memories. Very recently we have also been taking a preliminary (feasibility) look at cryogenic magnetoresistive memories.

SUMMARY OF PROGRESS OVER THE PAST YEAR AND FUTURE PLANS

Kinetic Inductance Memory Cell. During the past year we have received the test cells fabricated by TRW. Working with TRW, we have developed automated testing procedures and undertaken preliminary tests. The functionality of the circuits has been demonstrated, but they did not function completely as expected. It is not clear at this point whether the problem is one of design or new test equipment. The testing of these circuits will be completed in the near future.

Ferromagnetic Cores. A report describing this concept has been completed as part of an undergraduate honors thesis at Stanford. The student won a Hertz Fellowship and went on to graduate school. A patent disclosure has been submitted on this concept. The next step in exploring this approach involves detailed materials studies. We are not planning to carry out such studies at the present time.

Semiconducting/Superconducting Hybrids. The low operating temperature of such a semiconductor system means that a circuit will operate faster than its room-temperature cousin. However it also means that each mW of power is much more expensive to remove. This is unfortunate, since the power of a CMOS system does not scale as the temperature is lowered. In fact, since the circuit runs faster, it actually dissipates more power. A semiconductor memory for a superconducting system needs to meet two conflicting constraints—fast access time, and low power dissipation. The fastest semiconductor memories currently use bipolar transistors (BiCMOS) and dissipate many watts. They are not a solution for cryogenic operation.

Consequently, we are investigating fast, low power CMOS memories. Since power in CMOS technology is mostly from charging and discharging capacitance, the easiest way to reduce the power is to reduce the supply voltage. Low temperature operation means that the sub-threshold leakage is very small, and so threshold voltages and power-supplies can be greatly reduced. At about 2V supply voltage, the power of a 64 kbit memory should be under 100mW, which should be manageable. The problem is to make the memory fast enough.

The delay in a CMOS memory has two major components. One is the time required to decode the address and drive the correct wordline, and the other is the time needed to sense the value that the cell is driving on the bitlines. While using superconducting technology might help with the sensing, as is being explored by the Berkeley group, it is unlikely it will help with the decoder time. The decoder and wordline drive generally take one-half of the access time, so it is a nontrivial consideration. We are looking at circuit techniques that will reduce this delay. While we have been making some progress we currently feel that with 0.5 μm CMOS technology it will be very hard to get the memory access time under a few ns without a new idea. We will be getting together with the Berkeley group to confirm these conclusions. We have already designed some CMOS-only sense circuits, and plan to look at superconducting/semiconductor sense alternatives next. We plan to carry out detailed simulations of these approaches using CMOS device models adequate to describe cryogenic operations.

Another problem in the semiconducting/superconducting hybrid approach is the need to amplify the low signal levels of JJ circuits sufficiently to drive semiconductor circuits. One proposed approach to this problem is the flux flow transistor. Some controversy has developed over this concept due to the difficulties experienced by many groups to reproduce the results. Most of these studies have involved complicated material such as NbN and the high T_c superconductors. In order to clarify the issues we fabricated some flux flow transistors using as model materials, amorphous Mo-Ge alloys. These alloys are under excellent materials control in our laboratory. They have low pinning, very high sheet resistances and large superconducting penetrations depths—all good attributes for flux flow transistors. We were unable to get any active control of the device other than through simple heating effects associated with the control line going normal. In fact thermal runaway dominated the behavior of the devices except very near T_c . We found these heating effects to be in accord with classic theories of heating effects in superconducting bridges worked out by us many years ago. We note, however, that such classical heating effects will be much less important in high- T_c devices, because the thermal boundary conductance is much increased (by a factor of 1000) at these higher temperatures. We do not plan to continue this work but rather to consider other solutions to the driver circuit problem.

Another approach to semiconductor driver circuits is series arrays of Josephson junctions with a common input drive inductor. The idea is that one gets n times the output of a single junction (or SQUID). The theory for such structures is trivial for high capacitance (high beta-c) junctions, in which the ac Josephson currents are internally shunted by this large capacitance, but the device is hysteretic. For low beta-c junctions the I-V curves are not hysteretic, but one has to consider where the ac Josephson currents go. The situation is very close to that encountered in circuits used to make local oscillators out of series arrays of Josephson junctions. The critical issue is whether the junction oscillations lock in phase or in an anti-phase configuration. The I-V curves are completely different in these two cases. Transitions between the two are possible as a function of bias current. Chaos can also arise. We have previously studied such phase locking of Josephson arrays in a local oscillator context. With a new student, we are adapting the techniques used in our earlier work to this new problem.

Hybrid Magnetoresistive memories. In our original proposal for this program, we considered examination of the possible utility of magnetoresistive memory arrays for use with Josephson junction logic. Recent advances in magnetoresistive memory arrays, as a kind of nonvolatile all-solid-state "disk" memory, have attracted considerable attention. We are in the process of rethinking the possible utility of these memories for cryogenic use. The needed magnetic field and current levels seem compatible. The use of superconducting sense circuits may permit faster access, as they do in CMOS. We plan to continue this work sufficiently to establish whether a full-fledged study would be warranted.

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